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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION
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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,015	RUDECK ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *04102002* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 7 and 8 are objected to on the basis of presentation and form. Claim 7 represents a definition of the terms, *height* and *width*, whereas Claim 8 provides a limitation on the two "lengths," as defined. It would be clearer and more uniform if the two claims were combined.

2. Claims 9 – 12 are objected to on the basis of lack of definiteness. There is ambiguity in the claims and Examiner has had difficulty in interpreting the claim limitations because of the lack of clarity. Clarification or a change in the claim language is required.
The phrases of concern include the following: a) Claim 9 – *"one or more horizontal Surfaces planar to the substrate having a desired doping concentration," "the one or more vertical surfaces having a lower than desired doping concentration,"* and *"one or more vertical phosphorous-doped oxide layers having an additional doping concentration,"* b) Claim 10 – *"wherein the additional doping concentration and the less than desired doping concentration produce an effective doping concentration,"* c) Claim 11 – *"wherein the effective doping concentration is substantially equal to the desired doping concentration,"* d) Claim 12 – *"wherein the additional doping concentration, the less than desired doping concentration and the desired doping concentration are selected to provide a desired resistance."*

Claim Rejections – 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US 6,657,893 B2) in view of Wu (US 6,649,308 B1) and Colabella (US 6,252,274 B1).

5. Regarding Claim 1, Takahashi et al. disclose (Col. 21, lines 10 – 50) a semiconductor device comprising a substrate (1) (Figure 1), source/drain regions (8,9,10), a first oxide layer (4), a first polysilicon layer (5) deposited over the first oxide layer, a second oxide layer (6) deposited over the first polysilicon layer and a second polysilicon layer (7) deposited over the second oxide layer.

Takahashi et al. do not disclose the presence of a self aligned source. Colabella discloses the use of the self aligned source (SAS) procedure (Col. 5, lines 22 – 44) for memory devices. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the SAS procedure of Colabella with Takahashi et al. to make leakage currents less likely to occur (Col. 4, lines 2 – 4, Colabella)

Additionally, Takahashi et al. do not disclose the presence of a phosphorous-doped oxide along the vertical edges of the gate stack. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the

time of the invention to use the phosphorous-doped oxide (PSG) spacers in Takahashi et al. to provide a dopant source for drive in to form extended source and drain regions (Col. 4 lines 60 – 65, Wu).

6. Regarding Claim 2, Takahashi et al. disclose that the first oxide layer (4) is a tunnel oxide layer (Col. 36, lines 53 – 57).

7. Regarding Claim 3, Takahashi et al. do not disclose that an oxide-nitride-oxide (ONO) layer is formed atop the first polysilicon layer as the second oxide layer, however, Colabella discloses the formation of an ONO structure atop the first polysilicon layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the ONO structure of Colabella with Takahashi et al. to obtain a semiconductor device with low leakage currents and high voltage breakdown.

8. Regarding Claim 4, Takahashi et al. disclose that the first polysilicon layer (5) is a floating gate (Col. 21, lines 16 – 18).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Wu and Colabella, as applied to Claims 1 – 4, and further in view of Sung et al. (US 6,417,049 B1).

10. Regarding Claim 5, Takahashi et al. do not explicitly disclose the presence of word-lines formed from the second polysilicon layer. Sung et al. disclose (Col. 3, lines 43 – 48) that the second polysilicon layer (control gate) (19) (Figure 1f) form a wordline (WL).
It would have then been obvious to combine Sung et al. with Takahashi et al., Wu, and

Colabella to form an interconnected working device.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colabella in view of Wu and Rodder (US 6,329,225 B1).

12. Regarding Claim 6, Colabella discloses a semiconductor device after re-oxidation, where in the device comprises a substrate (1) (Figures 1, 2A, 3), a drain (self aligned) and source (self aligned) (8,9), a first oxide (2) , a first polysilicon layer (4) over the first oxide, a second oxide (5) deposited over the first polysilicon layer, a second polysilicon layer (6) deposited over the second oxide layer, and spacers deposited along vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second polysilicon layer.

Colabella does not disclose that the spacers consist of phosphorous-doped oxide. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/ nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the phosphorous-doped oxide (PSG) spacers in Wu. to provide a dopant source for drive in to form extended source and drain regions (Col. 4, lines 60 – 65, Wu) in Colabella.

Colabella further does not disclose the re-oxidation profile. Rodder discloses (Col.5, lines 43 - 46) (Figure 2A) the reoxidation profile (layer 128) over the semiconductor device surface and having a height and width after formation. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Rodder with Colabella and Wu to ascertain an oxide layer profile subsequent to oxidation exposure.

13. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colabell in view of Wu and Rodder, as applied to Claim 6, and further in view of Liu et al. (US 5,094,984) and Sobek et al. (US 6,268,624 B1).

Colabella does not disclose the structure developed at the polysilicon/oxide interfaces subsequent to reoxidation or the dependency on properties of the phosphorous-doped oxide (PSG) Sobek et al. disclose (Col. 2, lines 1 - 17) (Figure 1) that the re-oxidation process, results in inter layer encroachment and the development of "cuspate" structure characterized by a "height" and a "width."

As discussed above, the use of the PSG spacers disclosed by Wu will provide isolation and a diffusion source in Colabella. Liu et al. disclose that (Col. 1, line 65 through Col. 2, line 2) PSG films are porous and highly hygroscopic, depending on the phosphorous concentration. Hence, the propensity for PSG films to trap diffusing water vapor or oxygen during oxide layer growth to reduce encroachment or cuspate layer development will be dependent on the characteristics of the PSG layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Liu et al. and Sobek et al. with Wu, Rodder and Colabella to obtain a device with reduced or suppressed oxygen or water vapor absorption at the edges of gate structure during re-oxidation processes.

14. Claims 9 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colabella in view of Wu.

15. Regarding Claims 9 –12, Colabella discloses a self aligned source of a flash memory device on a substrate, comprising one or more doped horizontal surfaces planar to the substrate (Figures 1A,3A) (source, 6, 4), one or more (low doped) vertical surfaces coupled to th horizontal surfaces (edges of 6, 4 and spacer) and spacers formed at the lateral edges of the gate stack.

Colabella does not disclose the presence of phosphorous-doped oxide spacers formed over the vertical surface areas of the gate structure. Wu discloses the presence of phosphorous-doped oxide spacers (16) (Figure 16) formed over the vertical surfaces of the gate structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the P-doped oxide spacers of Wu in Colabella to obtain gate isolation and improve short channel effect (Col. 5, lines 2 – 4, Wu).

16. Claim 13 is rejected under 35 U.S.C. 103(a) over Madurawe et al. (US 6,646,919 B1) in view of Colabella, Wu and Han et al.

17. Regarding Claim 13, Madeurawe et al. disclose a computer (or data processing system) (Col. 15, line 60 through Col. 16, line 4) (Figure 13) comprising a processor (1304), a system bus (1310) and a flash memory device (1306) coupled to the system bus (1310), wherein the cells of the memory component comprise a substrate (1) (Figures 1, 2A, 3), a drain (self aligned) and source (self aligned) (8,9), a first oxide (2) , a first polysilicon layer (4) over the first oxide, a second oxide (5) deposited over the first polysilicon layer, a second polysilicon layer (6) deposited over the second oxide layer, and spacers deposited along vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second

polysilicon layer.

Colabella does not disclose that the spacers formed on the vertical edges of the gate stack consist of phosphorous-doped oxide. Wu discloses (Col. 4, lines 28 – 36) the presence of a phosphorous-doped oxide (16) (Figure 8) along the vertical edges of an oxide/poly/ nitride stack (Figure 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the phosphorous-doped oxide (PSG) spacers in Wu. to provide a dopant source for drive in to form extended source and drain regions (Col. 4, lines 60 – 65, Wu) in Colabella.

Colabella further does not disclose the re-oxidation profile. Han et al. disclose (Figure 7) the reoxidation profile (layer 170) over the semiconductor device surface and having a height and width after formation. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Han et al. with Colabella and Wu to ascertain an oxide layer profile subsequent to oxidation exposure.

Conclusions

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(703) 308-1690.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
December 4, 2003

Steven Loke